WHAT IS CLAIMED IS:

1. A second order modulator circuit, comprising:

an input node Vin;

a signal node Vx;

an output node Yout

a first signal processing circuit block with a transfer function (H3) and an input and output;

a second signal processing circuit block with a transfer function (H2*H3) and an input and output;

the signal node Vx being coupled to the input of the first signal processing circuit block and the input of the second signal processing circuit block;

a first, second, third and fourth summing nodes;

a first buffer "a" with an input and output, the input of the first buffer "a" being adapted to receive input signal Vin, the output of the first buffer "a" being coupled to the first summing node;

the output of the first signal processing circuit block being coupled to the third summing node;

the output of the second signal processing circuit block being coupled to the fourth summing node;

an n-bit quantizer with an input and output;

the quantizer output being coupled to the fourth summing node;

a first integrator circuit with a transfer function (H1) and an input and output;

a second buffer "b" with an input and output, the input of the second buffer being coupled to the output of the first integrator, the output of the second buffer "b" being coupled to the second summing node;

the second summing node being coupled to the third summing node;

a second integrator circuit with a transfer function (H2) and an input and output;

the input of the second integrator being coupled to the third summing node;

the output of the second integrator being coupled to the input of the quantizer;

a first m-bit DAC with an input and output;

a second m-bit DAC with an input and output;

a third buffer "c" with an input and output, the input of the third buffer being coupled to the output of the first DAC, the output of the third buffer "c" being coupled to the first summing node;

a fourth buffer "d" with an input and output, the input of the fourth buffer "d" being coupled to the output of the second DAC, the output of the fourth buffer "d" being coupled to the second summing node;

the output of the first signal processing circuit block being coupled to the third summing node;

the fourth summing node coupled to the output node Yout;

the circuit output Yout being coupled to the input of the first DAC and the input to the second DAC completing a feedback loop;

the first DAC and third buffer "c" forming a feedback loop to the first integrator from Yout;

the second DAC and fourth buffer "d" forming a feedback loop to the second integrator from Yout; and

the quantizer swing reduction circuit operable to keep the input/output swing of the quantizer within the limit of finite quantization levels.

2. The circuit of Claim 1, further comprising a signal generator operable to output signal Vx.

3. The circuit of Claim 2 wherein output of the first integrator, the output of the second integrator, the output of the quantizer and the output signal Yout are:

$$Y1 = Vin \cdot \left(\frac{H1 \cdot H2}{1 + H1 \cdot H2 + d \cdot H2}\right) \cdot \left(\frac{1}{H2} + d\right) - \varepsilon_q \cdot \left(\frac{H1}{1 + H1 \cdot H2 + d \cdot H2}\right) \quad [5]$$

$$Y2 = Vin \cdot \frac{H1 \cdot H2}{1 + H1 \cdot H2 + d \cdot H2} - \varepsilon_q \cdot \left(\frac{H1 \cdot H2 + d \cdot H2}{1 + H1 \cdot H2 + d \cdot H2}\right) - Vx \cdot H2 \cdot H3 \quad [6]$$

$$Y3 = Vin \cdot \frac{H1 \cdot H2}{1 + H1 \cdot H2 + d \cdot H2} + \varepsilon_q \cdot \left(\frac{1}{1 + H1 \cdot H2 + d \cdot H2}\right) - Vx \cdot H2 \cdot H3 \quad [7]$$

$$Yout = Vin \cdot \frac{H1 \cdot H2}{1 + H1 \cdot H2 + d \cdot H2} + \varepsilon_q \cdot \left(\frac{1}{1 + H1 \cdot H2 + d \cdot H2}\right) \quad [8]$$

4. The circuit of Claim 1, wherein the modulator output signal Yout is coupled to signal node Vx such that Yout, equals Vx.

5. The circuit of Claim 4, wherein the first integrator does not have delay;

the second integrator has delay; and

all the gain co-efficients of the first, second, third and fourth buffers equal unity.

6. The circuit of Claim 4, wherein the first signal processing circuit block has a transfer function (H3) of ((1-(1/Z))/(1));

the first integrator circuit has a transfer function (H1) of ((1)/(1-(1/Z)));

the second integrator circuit has a transfer function (H2) of ((1/Z)/(1-(1/Z))); and

the second signal processing circuit block has a transfer function (H2*H3) of ((1/Z)/(1)).

7. The circuit of Claim 6 wherein output of the first integrator, the output of the second integrator, the output of the quantizer and the output signal Yout are, respectively:

$$Y1 = Vin - \varepsilon_q \cdot \left(1 - Z^{-1}\right) \quad [10]$$

$$Y2 = Vin \cdot Z^{-1} \cdot \left(1 - Z^{-1}\right) + \varepsilon_q \cdot \left[\left(1 - Z^{-1}\right)^3 - 1\right] \quad [11]$$

$$Y3 = Vin \cdot Z^{-1} \cdot \left(1 - Z^{-1}\right) + \varepsilon_q \cdot \left(1 - Z^{-1}\right)^3 \quad [12]$$

$$Yout = Vin \cdot Z^{-1} + \varepsilon_q \cdot \left(1 - Z^{-1}\right)^2 \quad [13]$$

8. The circuit of Claim 4, wherein the modulator output signal Yout is coupled to signal node Vx such that Yout, equals Vx;

the first integrator has delay;

the second integrator has delay;

the gain co-efficients of the first and second buffers equal ½; and

the gain co-efficients of the third and fourth buffers equal unity.

9. The circuit of Claim 4, wherein the first signal processing circuit block has a transfer function (H3) of ((1-(1/Z))/(1));

the first integrator circuit has a transfer function (H1) of ((1/Z)/(1-(1/Z)));

the second integrator circuit has a transfer function (H2) of ((1/Z)/(1-(1/Z))); and

the second signal processing circuit block has a transfer function (H2*H3) of ((1/Z)/(1)).

10. The circuit of Claim 9 wherein output of the first integrator, the output of the second integrator, the output of the quantizer and the output signal Yout are, respectively:

$$Y1 = \frac{1}{2} \cdot \left[Vin \cdot Z^{-1} \cdot \left(1 + Z^{-1}\right) - \varepsilon_q \cdot Z^{-1} \cdot \left(1 - Z^{-1}\right) \right] \quad [14]$$

$$Y2 = Vin \cdot Z^{-2} \cdot \left(1 - Z^{-1}\right) + \varepsilon_q \cdot \left| \left(1 - Z^{-1}\right)^3 - 1 \right| \quad [15]$$

$$Y3 = Vin \cdot Z^{-2} \cdot \left(1 - Z^{-1}\right) + \varepsilon_q \cdot \left(1 - Z^{-1}\right)^3 \quad [16]$$

$$Yout = Vin \cdot Z^{-2} + \varepsilon_q \cdot \left(1 - Z^{-1}\right)^2 \quad [17]$$

11. The circuit of Claim 1 for use in a high speed analog to digital converter.

12. The circuit of Claim 1 wherein the first DAC and second DAC are implemented as an array of finite capacitors configured such that a selected number of these capacitors release their electrical charge into a summing junction that produces an equivalent analog output signal of the m-bit digital input code.

13. The circuit of Claim 1, further comprising an analog filter coupled between the input node Vin and the input of the first buffer "a".

14. The circuit of Claim 1 operable to permit a larger input/output swing range without degrading the SNR and SFDR performance due to quantizer saturation and clipping.

15. A second order modulator circuit, comprising:

an input node Vin;

a signal node Vx;

an output node Yout;

the signal node Vx and output node Yout coupled such that Vx equals Yout;

a first signal processing circuit block with a transfer function (H3) and an input and output;

a second signal processing circuit block with a transfer function (H2*H3) and an input and output;

the signal node Vx being coupled to the input of the first signal processing circuit block and the input of the second signal processing circuit block;

a first, second, third and fourth summing nodes;

a first buffer "a" with an input and output, the input of the first buffer "a" being adapted to receive input signal Vin, the output of the first buffer "a" being coupled to the first summing node;

the output of the second signal processing circuit block being coupled to the fourth summing node;

an n-bit quantizer with an input and output;

the quantizer output being coupled to the fourth summing node;

a first integrator circuit with a transfer function (H1) and an input and output;

a second buffer "b" with an input and output, the input of the second buffer being coupled to the output of the first integrator, the output of the second buffer "b" being coupled to the second summing node;

a second integrator circuit with a transfer function (H2) and an input and output;

the second summing node being coupled to input of the second integrator;

the output of the second integrator being coupled to the input of the quantizer;

a first m-bit DAC with an input and output;

a second m-bit DAC with an input and output;

a third buffer "c" with an input and output, the input of the third buffer "c" being coupled to the output of the first DAC, the output of the third buffer "c" being coupled to the first summing node;

a fourth buffer "d" with an input and output, the input of the fourth buffer "d" being coupled to the output of the second DAC, the output of the fourth buffer "d" being coupled to the second summing node;

a fifth buffer "1/d", with an input and output, the output of the first signal processing circuit block being coupled to the fifth buffer "1/d" input;

the fifth buffer "1/d" output being coupled to the third summing node;

the fourth summing node being coupled to the output node Yout;

the circuit output Yout being coupled to the input of the first DAC and the third summing node;

the third summing node being coupled to the input to the second DAC completing a feedback loop;

the first DAC and third buffer "c" forming a feedback loop to the first integrator from Yout;

the second DAC and fourth buffer "d" forming a feedback loop to the second integrator from Yout and the first signal processing circuit block (H3); and

the quantizer swing reduction circuit operable to keep the input/output swing of the quantizer within the limit of finite quantization levels.

16. The circuit of Claim 15 for use in a high speed analog to digital converter.

17. The circuit of Claim 15, further comprising the signal node Vx being coupled to the output node Yout such that Yout equals to signal Vx.

18. The circuit of Claim 15, further comprising an analog filter coupled between the input node Vin and the input of the first buffer "a".

19. The circuit of Claim 15 wherein the first DAC and second DAC are implemented as an array of finite capacitors configured such that a selected number of these capacitors release their electrical charge into a summing junction that produces an equivalent analog output signal of the m-bit digital input code.

20. The circuit of Claim 19 wherein the first DAC and the second DAC are operable to produce an equivalent analog output signal of the m-bit digital input code at a junction at the output of the first integrator and input of the second integrator.

21. The circuit of Claim 15 operable to permit a larger input/output swing range without degrading the SNR and SFDR performance due to quantizer saturation and clipping.

22. A sigma delta modulator circuit for use in an ADC, comprising:

at least a first and a second integrator, the input to the first integrator being coupled to an input signal source, Vin, and the output of the first integrator being coupled to the input of the second integrator;

at least one n-bit quantizer being coupled to the output of the second integrator;

at least one m-bit DAC;

the quantizer being enclosed in a feedback loop via the m-bit DAC;

the DAC is operable to produce an equivalent analog output signal of the m-bit digital input code at a junction at the output of the first integrator and input of the second integrator.

a quantizer swing reduction circuit coupled between the output of the quantizer and the input to the second integrator, operable to keep the input/output swing of the quantizer within the limit of the finite quantization levels.

23. The circuit of Claim 22 wherein the DAC is implemented as an array of finite capacitors configured such that a selected number of these capacitors release their electrical charge into a summing junction that produces an equivalent analog output signal of the m-bit digital input code.

24. The circuit of Claim 23 wherein the DAC is operable to produce an equivalent analog output signal of the m-bit digital input code at a junction at the output of the first integrator and input of the second integrator.

25. A quantizer swing reduction circuit, comprising:

an input signal generator with an output terminal operable to output a signal Vx;

a first signal processing circuit block with a transfer function (H3) and an input and output terminal;

a second signal processing circuit block with a transfer function (H2*H3) and an input and output terminal;

the output terminal of the input signal generator being coupled to the input of the first signal processing circuit block and the input of the second signal processing circuit block;

the output of the first signal processing circuit block being coupled to an output of a first integrator; and

the output of the second signal processing circuit block being coupled to an output of a quantizer.

26. The quantizer swing reduction circuit of Claim 25 further comprising:

at least one integrator circuit;

a quantizer circuit;

a feedback DAC circuit coupling the quantizer to the integrator circuit;

the quantizer swing reduction circuit being coupled between the output of the quantizer circuit and the input to an integrator; and

said quantizer swing reduction circuit operable to keep the input/output swing of the quantizer within the limit of the finite quantization levels.

27. The circuit of Claim 26 wherein the quantizer circuit consists of an array of finite comparators in parallel such that each comparator compares the analog signal at the quantizer input to a reference voltage associated to its own output level;

28. The circuit of Claim 27 wherein the reference voltage for each comparator in the array is equally spaced by the number of comparators in the array within the A/D positive full-scale and negative full-scale;

a common clock latch/triggers the output of the comparators, such that each comparator generates a logic "high" (1) or a logic "low" (0) level, with the parallel output of the comparator representing a digital code equivalent to the analog signal at the quantizer input;

the code being digitally processed to generate an n-bit digital word representing the converted analog signal that is the output of the modulator and also fed back into a analog filter loop via the feedback DAC;

the error between the modulator analog input signal and the modulator digital output code due to the quantizer is the quantization noise

29. A modulator circuit, comprising:

an input node Vin;

a signal node Vx;

an output node Yout

a first signal processing circuit block with a transfer function (H3) and an input and output;

a second signal processing circuit block with a transfer function (H2*H3) and an input and output;

the signal node Vx being coupled to the input of the first signal processing circuit block and the input of the second signal processing circuit block;

a first, second and third summing nodes;

a first buffer "a" with an input and output, the input of the first buffer "a" being adapted to receive input signal Vin, the output of the first buffer "a" being coupled to the first summing node;

the output of the first signal processing circuit block being coupled to the second summing node;

the output of the second signal processing circuit block being coupled to the third summing node;

an n-bit quantizer with an input and output;

the quantizer output being coupled to the third summing node;

an integrator circuit with a transfer function (H1) and an input and output;

the output of the integrator being coupled to the input of the quantizer;

an m-bit DAC with an input and output;

a second buffer "b" with an input and output, the input of the second buffer being coupled to the output of the DAC, the output of the second buffer "b" being coupled to the first summing node;

the output of the first signal processing circuit block being coupled to the second summing node;

the third summing node coupled to the output node Yout;

the circuit output Yout being coupled to the input of the DAC completing a feedback loop;

the quantizer swing reduction circuit operable to keep the input/output swing of the quantizer within the limit of finite quantization levels.

30. The circuit of Claim 29, wherein output signal, Yout is coupled to signal node Vx, such that Yout equals Vx;

the integrator having a delay; and

the gain co-efficients of the first and second buffers equal unity.

31. The circuit of Claim 29, wherein the first signal processing circuit block has a transfer function (H3) of ((1-(1/Z))/(1));

the integrator has a transfer function (H1) of ((1/Z)/(1-(1/Z))); and

the second signal processing circuit block has a transfer function (H2*H3) of ((1/Z)/(1)).

32. The circuit of Claim 31 wherein output of the integrator, the output of the quantizer and the output signal Yout are, respectively:

$$Y2 = Vin \cdot Z^{-1} \cdot \left(1 - Z^{-1}\right) + \varepsilon_q \cdot \left[\left(1 - Z^{-1}\right)^2 - 1\right] \quad [18]$$

$$Y3 = Vin \cdot Z^{-1} \cdot \left(1 - Z^{-1}\right) + \varepsilon_q \cdot \left(1 - Z^{-1}\right)^2 \quad [19]$$

$$Yout = Vin \cdot Z^{-1} + \varepsilon_q \cdot \left(1 - Z^{-1}\right) \quad [20]$$